WHAT IS CLAIMED IS

1. A process of fabricating a high resistance CMOS resistor, comprising the steps of:

providing a p-type silicon substrate;

forming an n-well in said p-type silicon substrate;

forming a p-well in a non-active area of said p-type silicon substrate;

forming a pad oxide layer on the surface of said p-type silicon substrate;

forming a first p-field region into said p-well and a second p-field region into said n-well, wherein said second p-field region forms a CMOS resistor;

forming a field oxide layer over said CMOS resistor;

forming an n-type contact region in said n-well;

forming two p-type contact regions respectively as a first ohmic contact and a second ohmic contact of said CMOS resistor respectively;

forming a patterned BPSG layer to build two contact openings exposing a portion of said n-type contact region and said two p-type contact regions;

forming two metal contact plugs in said contact openings to electrically connect to said first ohmic contact and said second ohmic contact of said CMOS resistor; and

depositing a passivation layer over said contact plugs covering said CMOS resistor.

2. The method of claim **1**, wherein said p-type silicon substrate is doped with boron ions, and has a resistance in a range of 8 Ω to 12 Ω per cm.

3. The method of claim **1**, wherein said n-well is formed by implanting phosphorus ions using an energy level of 100KeV, and with a dosage level in a range of $6x10^{12}$ to $9x10^{12}$ ions/cm^2.

4. The method of claim **1**, wherein said p-well is formed by implanting boron ions using an energy level of 40KeV, and with a dosage level in a range of 8×10^{12} to 9×10^{12} ions/cm^2.

5. The method of claim **1**, further comprising a step of performing a thermal annealing process at a temperature of 1150℃ for diffusing ions of said n-well and said p-well into respective regions in said p-type silicon substrate.

6. The method of claim **1**, wherein said pad oxide is grown to a thickness of 350 angstroms at a temperature of 900℃.

7. The method of claim **1**, further comprising a step of growing a nitride layer to a thickness of 1250 angstroms at a temperature of 850℃ and etching said nitride layer to form a patterned mask layer which serves as a mask for forming said first p-field region and said second p-field region.

8. The method of claim **1**, wherein said first p-field region and said second p-field region are formed by implanting boron ions using an energy level of 50KeV, and with a dosage level in a range of 4×10^{13} to 6×10^{13} ions/cm^2.

9. The method of claim **1**, wherein said field oxide layer is grown to a thickness of 5000 to 6000 angstroms by performing a thermal annealing process at a temperature of 980℃.

10. The method of claim **1**, wherein said n-type contact region is formed by implanting arsenic using an energy level of 80KeV, and with a dosage level of 4×10^{15} to 6×10^{15} ions/cm^2.

11. The method of claim **1**, wherein said two p-type contact regions are formed by implanting boron ions using an energy level of 25KeV, and with a dosage level of 2×10^{15} to 4×10^{15} ions/cm^2.

12. The method of claim **1**, wherein said metal contact plugs comprises AlSiCu.

13. The method of claim **1**, wherein said BPSG layer has a thickness in a range of 5000 to 8000 angstroms.

14. The method of claim **1**, wherein said passivation layer is an oxide layer having a thickness in a range of 5000 to 10000 angstroms.

15. The method of claim **1**, wherein said CMOS resistor has at least a resistance of 10 $k\Omega$ per square.

16. The method of claim **1**, wherein said process is compatible with a standard CMOS processes.